AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method comprising:

providing a wafer comprised of a bulk substrate, an insulating layer positioned above said bulk substrate, and a semiconducting layer positioned above said insulating layer;

forming an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate;

forming a patterned layer of photoresist above said exposed surface area of said bulk substrate;

performing at least one etching process to form an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate using said patterned layer of photoresist as a mask for said at least one etching process; and

forming a layer of material above said alignment mark and in said opening.

2. (Previously Presented) The method of claim 1, wherein providing a wafer comprised of a bulk substrate, an insulating layer positioned above said bulk substrate, and a semiconducting layer positioned above said insulating layer comprises providing a wafer comprised of a bulk substrate comprised of at least one of silicon, silicon nitride, gallium arsenide, and silicon germanium.

3. (Original) The method of claim 1, wherein providing a wafer comprises providing a wafer having a diameter of at least one of approximately 4 inches, 8 inches and 12 inches.

4. (Original) The method of claim 1, wherein forming an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate comprises performing at least one etching process to form an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate.

5. (Canceled)

6. (Original) The method of claim 1, wherein forming a layer of material above said alignment mark and in said opening comprises depositing a layer of material above said alignment mark and in said opening.

7. (Original) The method of claim 1, wherein forming a layer of material above said alignment mark and in said opening comprises forming a layer of material comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than approximately 8.0 above said alignment mark and in said opening.

8. (Original) The method of claim 1, further comprising performing a planarization operation after forming said material above said alignment mark and in said opening.

9. (Original) The method of claim 1, further comprising:

positioning said wafer in a photolithography stepper tool; and

reflecting a light off of said alignment mark formed in said bulk substrate to properly position said wafer for processing in said photolithography stepper tool.

10. (Original) The method of claim 1, wherein forming an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate comprises forming a plurality of openings in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate within each of said openings.

11. (Original) The method of claim 10, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate in each of said openings.

12. (Original) The method of claim 1, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark comprised of a plurality of grating structures in said bulk substrate within said exposed surface area of said bulk substrate.

13-43. (Canceled)

44. (New) The method of claim 1, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of silicon positioned above said insulating layer.

45. (New) The method of claim 1, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of gallium arsenide positioned above said insulating layer.

46. (New) The method of claim 1, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of silicon germanium positioned above said insulating layer.

47-59. (Canceled)